1Ω Dual SPDT Negative Signal Handing Analog Switch

General Description

The ET7428 is an advanced CMOS analog switch fabricated in Sub−micron silicon gate CMOS technology. The part also features guaranteed Break Before Make (BBM) switching, assuring the switches never short the driver. The switches can handle negative signal down to -3.6V. When the voltage of the COM terminal exceeds OVP threshold, the channels from the COM terminal to the NC and NO terminals will be turned off.

ET7428 is offered in a small QFN10L package, which is ideal for small form factor portable equipment.

Features

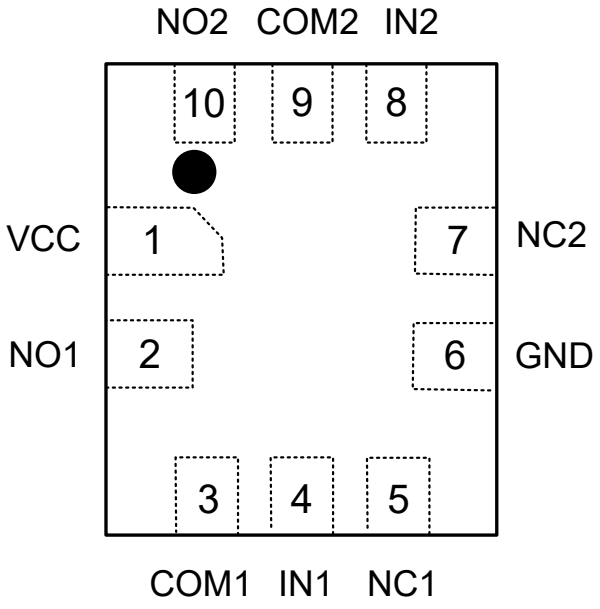
- Low R_{ON} is typical 1Ω @ V_{CC} =3.3V
- Single supply operation from 2.7V to 5.5V
- Full -3.6V to 5.5V signal handling capability
- High off-channel isolation
- Low standby current
- Low distortion
- Break-Before-Make (BBM) switching
- High continuous current capability is ±300mA through each switch
- Part No. and Package Information

Part No.	Package	Packing Option	MSL
ET7428	QFN10L (1.8mm × 1.4mm)	Tape and Reel ,3K	Level 1

Application

- Smart Phones and Cellular Phones
- Cell Phone Audio Block/ Speaker
- Earphone Switching Ring-Tone Chip
- Amplifier Switching/Modems

Pin Configuration



Top View

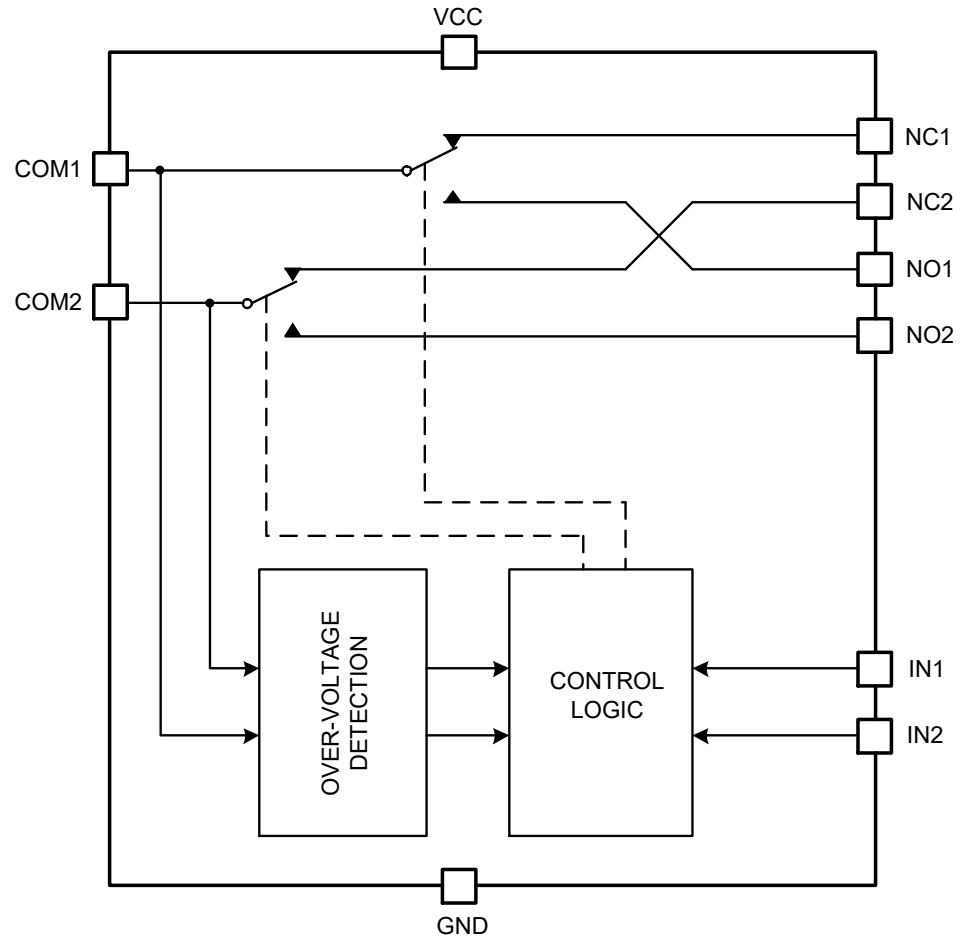
Pin Function

Pin NO.	Pin Name	Description
1	VCC	Power supply
2	NO1	Independent Channels
3	COM1	Common Channels
4	IN1	Controls
5	NC1	Independent Channels
6	GND	Ground (V)
7	NC2	Independent Channels
8	IN2	Controls
9	COM2	Common Channels
10	NO2	Independent Channels

Truth Table

Logic IN1/2	NO1/2 to COM1/2	NC1/2 to COM1/2
0	OFF	ON
1	ON	OFF

Analog Symbol



Analog Symbol

Absolute Maximum Ratings

Characteristic		Symbol	Value	Unit
Supply Voltage		V_{CC}	-0.5～+6.5	V
Analog Input Voltage(COM,NC,NO)		V_{IS}	-5～+12	V
Digital Select Input Voltage		V_{IN}	-0.5～+6.5	V
Continuous DC Current from COM to NC/NO		I_{AN1}	±300	mA
Peak Current from COM to NC/NO, 10 Duty Cycle (1)		I_{AN-PK1}	±500	mA
Storage Temperature		T_S	-55 to150	°C
ESD	Human Body Model(2)	HBM	2000	V
	Charge-Device Mode(2)	CDM	1500	V
Latch Up (Current Maximum Rating)(2)		I_{LATCH}	200	mA

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

Note1.Defined as 10% ON, 90% off duty cycle.

Note2.This device series incorporates ESD protection and is tested by the following methods:

ESD Human Body Model tested per ESDA/JEDEC JS-001-2017.

CDM tested per ESDA/JEDEC JS-002-2018.

Latch up Current Maximum Rating tested per JEDEC78.

Recommended Operating Conditions

Characteristic	Symbol	Min	Max	Unit
DC Supply Voltage	V_{CC}	2.7	5.5	V
Digital Select Input Voltage	V_{IN}	GND	5.5	V
Analog Input Voltage(COM1/2)	V_{IS}	-3.6	5.5	V
Analog Input Voltage(NC1/2, NO1/2)	V_{IS1}	-3.6	5.5	V
Operating Temperature Range	T_A	-40	+85	°C
Input Rise or Fall Time, SELECT	tr,tf	0	20	ns/V

Electrical Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IH}	High−Level Input Voltage, Select Inputs	V_{CC}=2.7V-5.5V	0.9			V
V_{IL}	Low−Level Input Voltage, Select Inputs	V_{CC}=2.7V-5.5V			0.4	V
V_{OVP_TH}	COM1/2 OVP positive threshold	V_{CC}=2.7V-5.5V	5.5	5.8	6.1	V
V_{OVP_HYS}	OVP threshold hysteresis	V_{CC}=2.7V-5.5V		200		mV
I_{IN}	Maximum Input Leakage Current, IN1/IN2	V_{CC} =5.5V V_{IN} =V_{CC} or GND			±0.3	uA
I_{CC}	Quiescent Supply Current	V_{CC} =3.3V IN1,2= 0V or V_{CC}		29		uA
I_{CCT}	Increase in I_{CC} per Input	V_{CC} =3.3V IN1=1.2V, IN2=0 or V_{CC}			55	uA
$I_{COM(ON)}$	COM ON leakage Current(4)	V_{CC}=5.5V,V_{COM} =5.5V V_{IN} = V_{IL} or V_{IH}, V_{NC} floating/V_{NO} floating			3	uA
R_{ON}	On−Resistance(4)	V_{CC} =3.3V V_{IS}=-3.6~5.0V I_{COM} = 100mA	0.7	1	1.3	Ω
R_{FLAT}	On−Resistance Flatness(4)(6)	V_{CC} =3.3V V_{IS}=-3.6~5.0V I_{COM} = 100mA			0.05	Ω
ΔR_{ON}	On−Resistance Match Between Channels(4)(5)	V_{CC} =3.3V V_{IS}=-3.6~5.0V I_{COM}=100mA			0.1	Ω
t_{ON}	Turn−On Time (Figure 1)	V_{CC} =3.3V V_{IS}=1.5V		25		us
		V_{CC} =3.3V V_{IS}=5.0V		35		
t_{OFF}	Turn−Off Time (Figure 1)	V_{CC} =3.3V V_{IS}=1.5V		1		us
		V_{CC} =3.3V V_{IS}=5.0V		1		
t_{BBM}	Break−Before−Make Time(Figure 2)	V_{CC} =3.3V, V_{IS}=1.5V C_L=35pF, R_L=50Ω		25		us
		V_{CC} =3.3V, V_{IS}=5V C_L=35pF, R_L=50Ω		35		

Electrical Characteristics (Continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
t_{DEB}	Debounce time (Figure 7)	V_{CC} =3.3V, V_{IS}=5.0V C_L=35pF, R_L=50Ω		7		ms
BW	On−Channel −3dB Bandwidth or Frequency Response(Figure 4) (3)	R_{IS}=50Ω		400		MHz
V_{ISO}	Off−Channel Isolation(3) (Figure 5)	V_{IS}=1V RMS F_{IS} = 100kHz V_{IN} =GND to V_{CC} C_L=5pF， R_L= 50Ω		-65		dB
Q	Charge Injection Select Input to Common I/O(3) (Figure 3)	V_{IN} = 0 or V_{CC} R_{IS}=0Ω,C_L=100pF R_L=1MΩ $Q=C_L×\Delta V_{Out}$		25		pC
THD	Total Harmonic Distortion THD +Noise(3)	V_{CC} =3.3V V_{IS}=1V RMS F_{IS}=20Hz to 20kHz R_L=50Ω,C_L=5pF		0.01		%
V_{CT}	Channel−to−Channel Crosstalk(3) (Figure 6)	V_{IS}=1V RMS F_{IS}= 100KHz, R_L= 50Ω,C_L=5pF		-70		dB
C_{IN}	ControlPin Input Capacitance(3)	V_{CC} =3.3V		4		pF
C_{NC}/C_{NO}	NC/NO Port Capacitance(3)	V_{CC} =3.3V		10		pF
C_{COM}	COM Port Capacitance When Switch is Enabled(3)	V_{CC} =3.3V		20		pF

Note3. Guaranteed by design

Note4. Guaranteed by design. Resistance measurements do not include test circuit or package resistance

Note5. $\Delta R_{ON} = R_{ON(NC1)} - R_{ON(NC2)}$ or $R_{ON(NO1)} - R_{ON(NO2)}$ when V_{IS} is same.

Note6. Flatness is defined as the difference between the maximum and minimum value of on−resistance as measured over the specified analog signal ranges.

Test Circuit

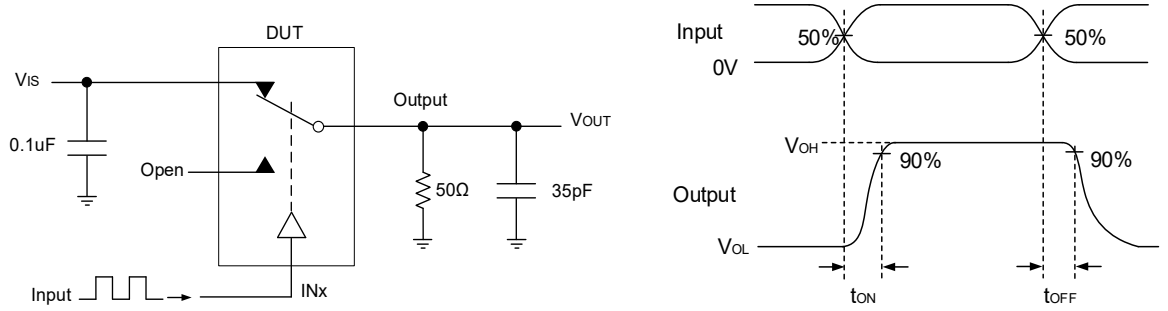


Figure1. t_{ON} /t_{OFF}

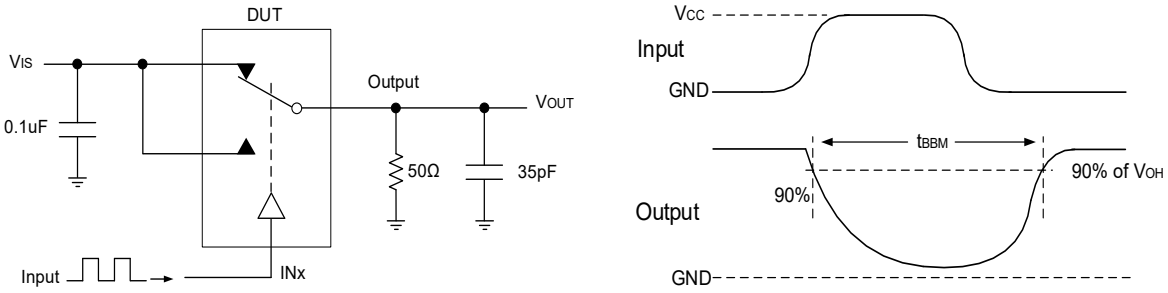


Figure2. t_{BBM}

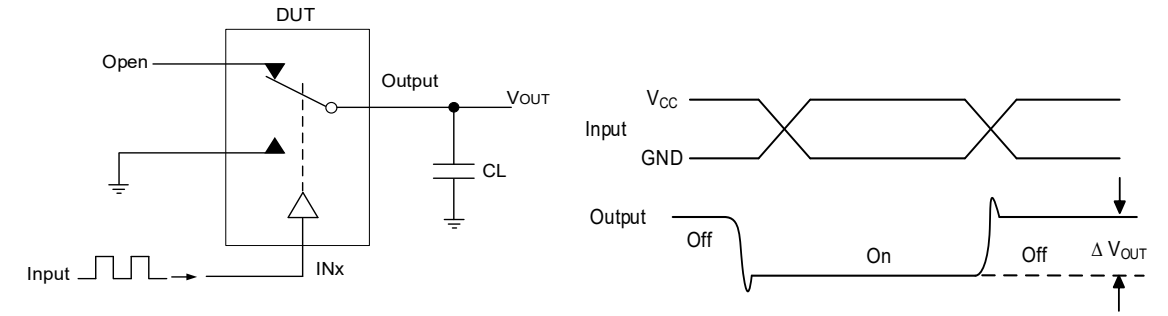


Figure3.Charge Injection

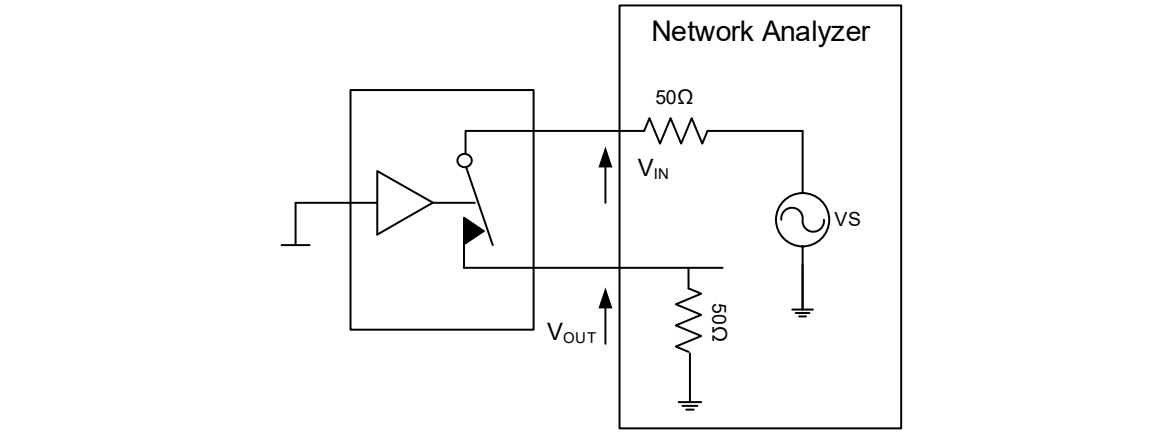
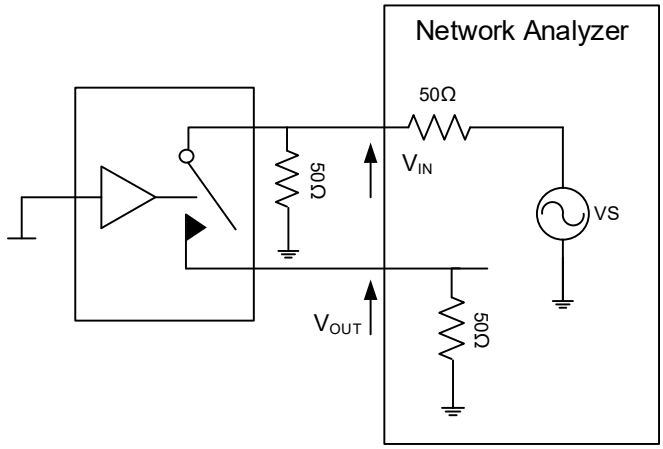


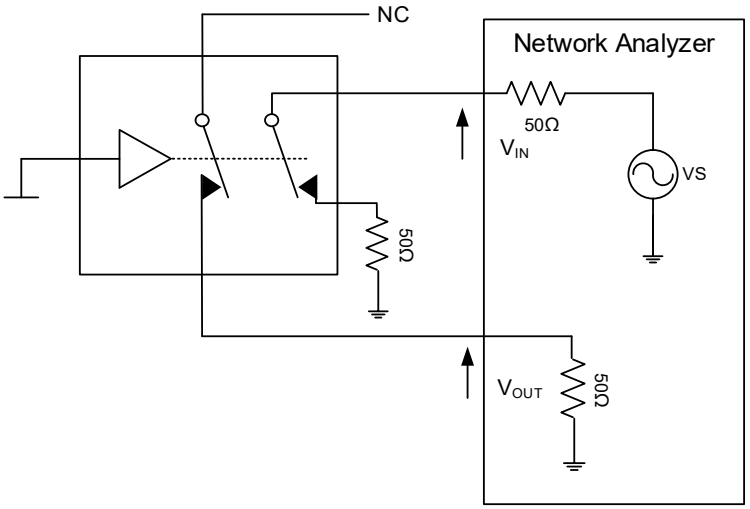
Figure4. Bandwidth

Test Circuit (Continued)



Off-Isolation=20 Log(V_{OUT}/V_{IN})

Figure5. Channel Off Isolation



CROSSTALK=20 Log($V_{OUT}/_{VIN}$)

Figure6. Non-Adjacent Channel-to-Channel Crosstalk

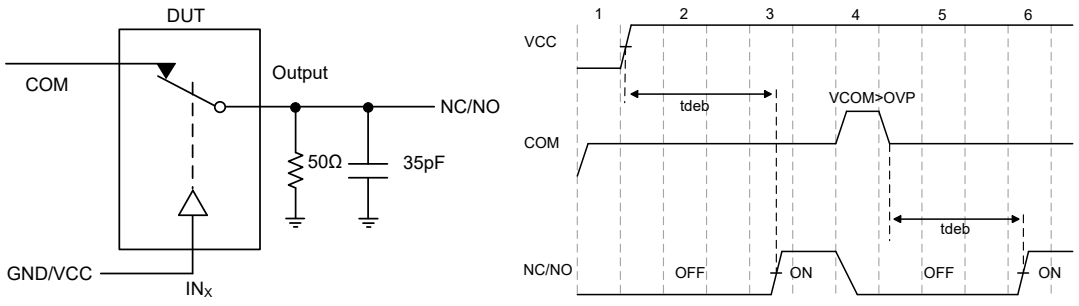
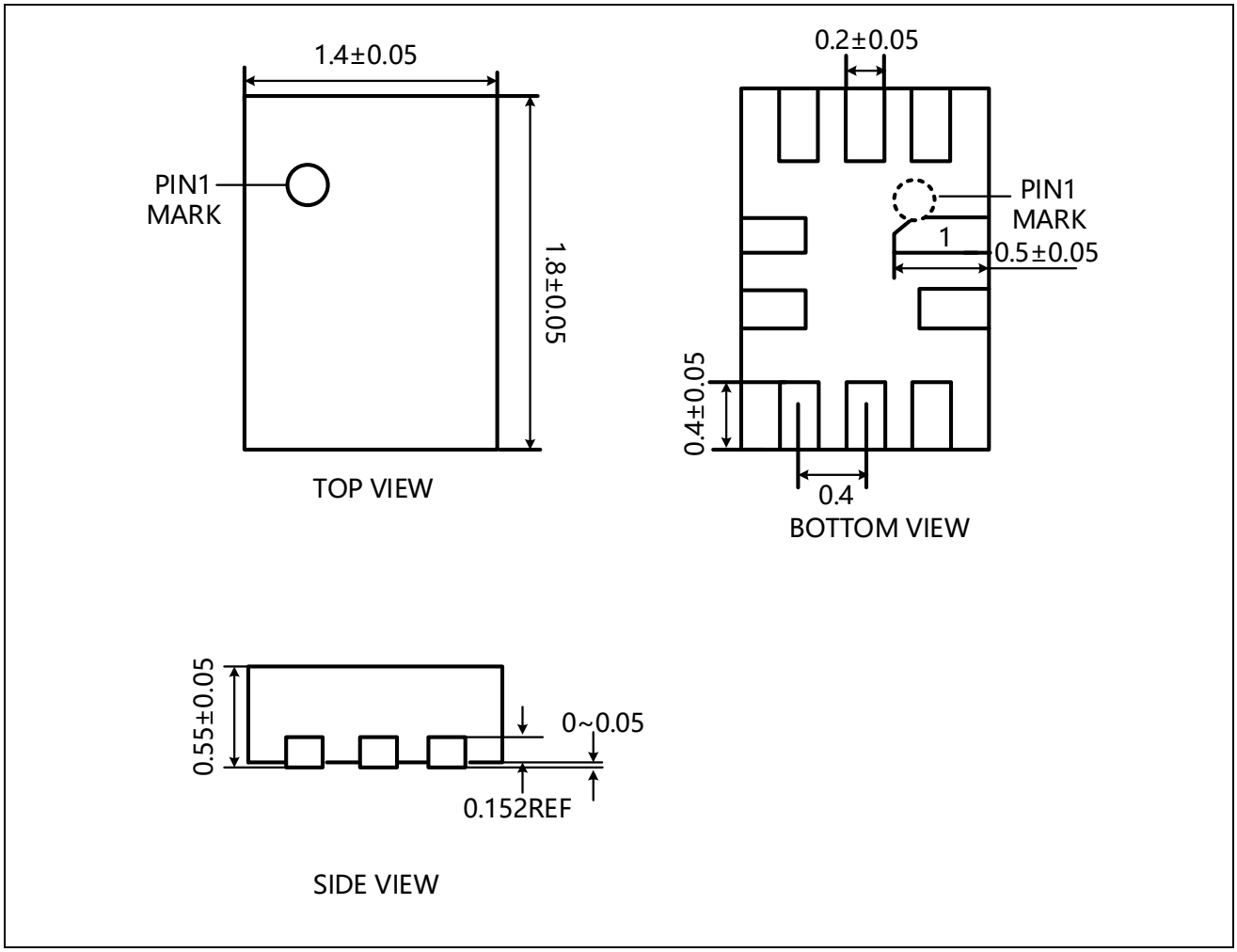


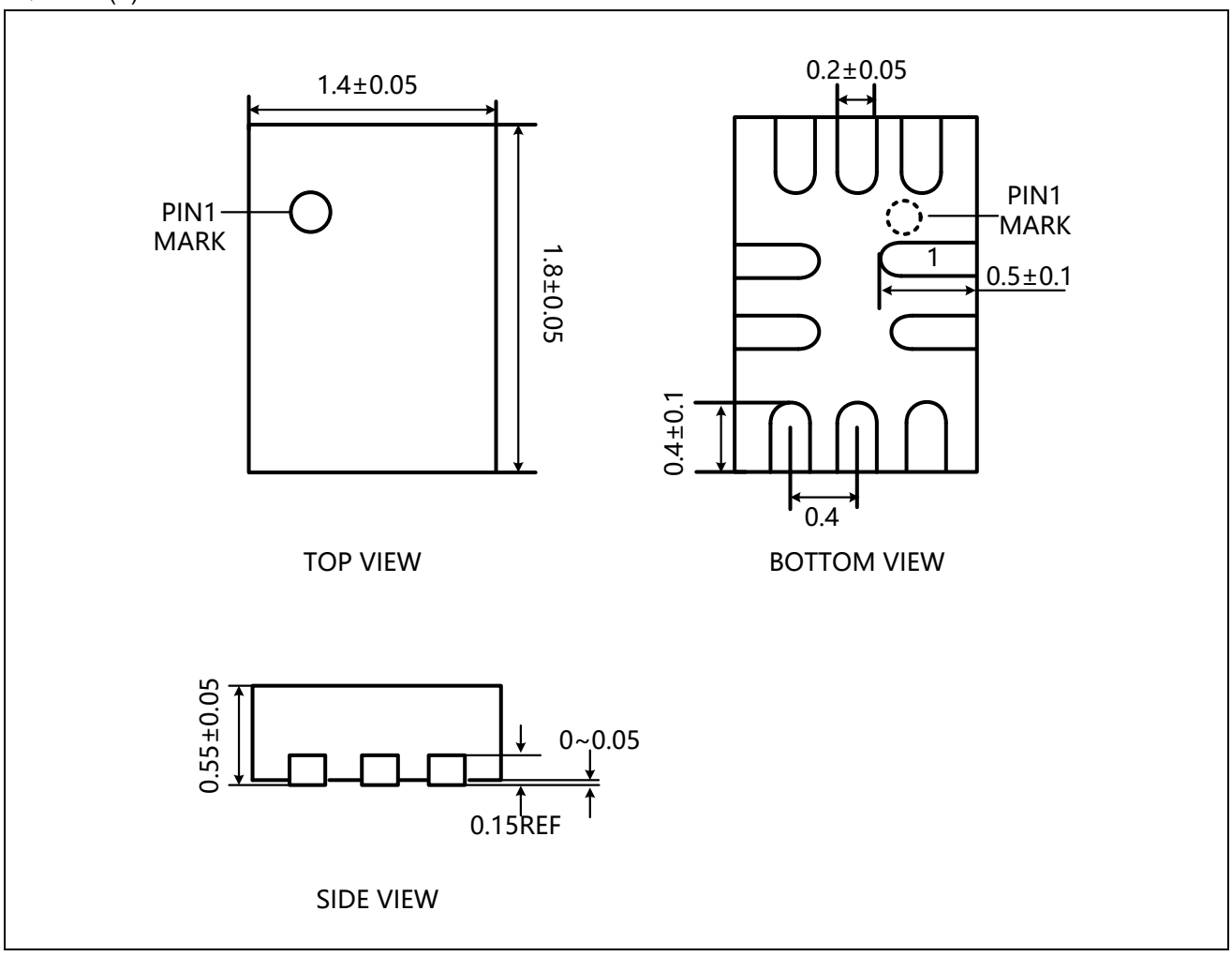
Figure7. t_{DEB}

Package Dimension

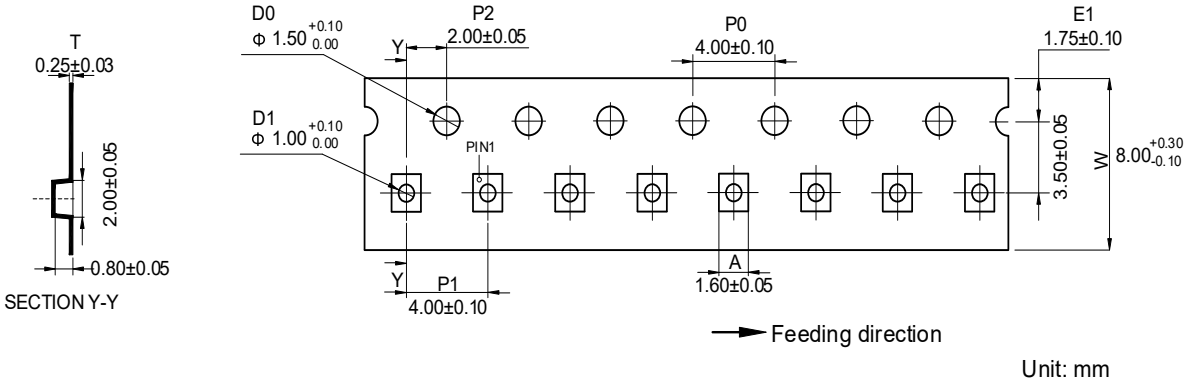
QFN10L(1)



QFN10L(2)

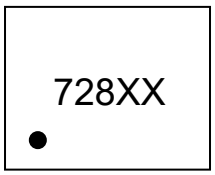

1.4±0.05
PIN1
MARK
1.8±0.05
TOP VIEW
0.2±0.05
PIN1
MARK
1
0.5±0.1
0.4±0.1
0.4
BOTTOM VIEW
0.55±0.05
0~0.05
0.15REF
SIDE VIEW

Tape Information



Marking Information

QFN10L



728 - Part Number

XX - Tracking Number

Note：XX(Tracking Number) is variable, according to the wafer lot number.

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2024-02-27	Original Version	Pansy	Wuxj	liujy
1.1	2025-10-28	Update Tape and Marking Information	Pansy	Wuxj	liujy